

In re Patent Application of
MARIAUD ET AL.
Serial No. 09/990,629
Filed: NOVEMBER 16, 2001

In the Claims:

This listing of claims replaces all prior versions or listings in the application.

Claims 1-6 cancelled.

7. (Previously presented) A control device, in a first peripheral apparatus, for controlling a first voltage applied to a first conductor wire of a universal serial bus (USB) in the first peripheral apparatus connected upstream to a second peripheral apparatus, the first peripheral apparatus comprising a supply voltage source for supplying the first voltage to the first conductor wire, and the first peripheral apparatus being connected to receive a second voltage on a second conductor wire of the USB, the control device comprising:

a detection circuit connected to the second conductor wire of the USB for detecting the second voltage received therefrom;

a memory connected to said detection circuit for storing a logic value corresponding to a presence or an absence of the second voltage; and

a logic control circuit connected to said memory for operating the supply voltage source only if the stored logic value indicates that the second voltage is present, to protect the second peripheral apparatus from receiving the first voltage via the first conductor wire of the USB of the first peripheral apparatus when the second voltage is not present.

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8. (Previously presented) A control device according to Claim 7, wherein said detection circuit comprises:

a Schmitt trigger having an input connected to the second conductor wire of the USB, and an output for providing an output signal;

an edge detection circuit connected to an output of said Schmitt trigger for detecting a rising edge or a falling edge of the output signal, and for producing at least one signal corresponding to the detected rising and falling edges of the output signal;

a counter connected to said edge detection circuit for counting a duration from which a logic value of the detected rising edge or of the detected falling edge of the output signal is maintained, and for producing an end of count signal when the counted duration reaches a predetermined value; and

a state machine connected between said edge detector and said counter for changing logic states as a function of the detected rising edge and the detected falling edge of the output signal and as a function of the end of count signal, said state machine producing a signal having a logic value corresponding to the presence or absence of the second voltage and for producing a signal indicating that the logic value corresponding to the presence or absence of the second voltage has changed.

9. (Previously presented) A control device according to Claim 7, further comprising a state register comprising at least one latch; and wherein said memory circuit comprises said at least one latch.

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10. (Previously presented) A control device according to Claim 7, wherein said logic control circuit comprises:

an inverter circuit having an input terminal for receiving the logic value corresponding to the presence or absence of the second voltage; and

a NOR circuit having a first input connected to an output terminal of said inverter circuit, and a second input for receiving a logic value indicating that the supply voltage source can be operated.

11. (Previously presented) A control device according to Claim 7, wherein the first peripheral apparatus comprises a microcontroller, an interrupt state register (ISR) for the microcontroller and comprising a plurality of latches, and an interrupt mask register (IMR) for the microcontroller and comprising a plurality of latches; the control device further comprising:

a circuit for interrupting the microcontroller and comprising

at least one latch from the ISR for recording a change in the logic value corresponding to the presence or absence of the second voltage,

at least one latch from the IMR for recording whether the microcontroller requires knowledge of the logic value recorded in said at least one latch from the ISR, and

an AND circuit having a first input connected to said at least one latch from the ISR and a second input connected to said at least one latch from the IMR, and an

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output for providing an interrupt request signal to the microcontroller only if there occurs a change in the logic value corresponding to the presence or absence of the second voltage and if the logic value recorded in said at least one latch from the ISR has a 1 logic value.

12. (Previously presented) A control device according to Claim 7, wherein the first conductor wire in the USB comprises a data conductor wire.

13. (Previously presented) A first peripheral apparatus connected upstream to a second peripheral apparatus via a universal serial bus (USB), the first peripheral apparatus comprising:

- a supply voltage source connected to a first conductor wire in the USB for supplying a first voltage thereto;

- a detection circuit connected to a second conductor wire of the USB for detecting a second voltage received therefrom;

- a memory connected to said detection circuit for storing a logic value corresponding to a presence or an absence of the second voltage; and

- a logic control circuit connected to said memory for operating said supply voltage source only if the stored logic value indicates that the second voltage is present, to protect the second peripheral apparatus from receiving the first voltage via the first conductor wire of the USB when the second voltage is not present.

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14. (Previously presented) A first peripheral apparatus according to Claim 13, wherein said detection circuit comprises:

a Schmitt trigger having an input connected to the second conductor wire of the USB, and an output for providing an output signal;

a edge detection circuit connected to an output of said Schmitt trigger for detecting a rising edge or a falling edge of the output signal, and for producing at least one signal corresponding to the detected rising and falling edges of the output signal;

a counter connected to said edge detection circuit for counting a duration from which a logic value of the detected rising edge or of the detected falling edge of the output signal is maintained, and for producing an end of count signal when the counted duration reaches a predetermined value; and

a state machine connected between said edge detector and said counter for changing logic states as a function of the detected rising edge and the detected falling edge of the output signal and as a function of the end of count signal, said state machine producing a signal having a logic value corresponding to the presence or absence of the second voltage and for producing a signal indicating that the logic value corresponding to the presence or absence of the second voltage has changed.

15. (Previously presented) A first peripheral apparatus according to Claim 13, further comprising a state

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register comprising at least one latch; and wherein said memory circuit comprises said at least one latch.

16. (Previously presented) A first peripheral apparatus according to Claim 13, wherein said logic control circuit comprises:

an inverter circuit having an input terminal for receiving the logic value corresponding to the presence or absence of the second voltage; and

a NOR circuit having a first input connected to an output terminal of said inverter circuit, and a second input for receiving a logic value indicating that said supply voltage source can be operated.

17. (Previously presented) A first peripheral apparatus according to Claim 13, further comprising:
a microcontroller;

an interrupt state register (ISR) for said microcontroller and comprising a plurality of latches;

an interrupt mask register (IMR) for said microcontroller and comprising a plurality of latches; and

a circuit for interrupting said microcontroller and comprising

at least one latch from said ISR for recording a change in the logic value corresponding to the presence or absence of the second voltage,

at least one latch from said IMR for recording whether said microcontroller requires knowledge of the logic value recorded in said at least one latch from said ISR, and

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an AND circuit having a first input connected to said at least one latch from said ISR and a second input connected to said at least one latch from said IMR, and an output for providing an interrupt request signal to said microcontroller only if there occurs a change in the logic value corresponding to the presence or absence of the second voltage and if the logic value recorded in said at least one latch from said ISR has a 1 logic value.

Claims 18-21. (canceled).

22. (Previously presented) A method for automatically controlling a first voltage being applied to a first conductor wire of a universal serial bus (USB) in a first peripheral apparatus connected upstream to a second peripheral apparatus, the first peripheral apparatus comprising a supply voltage source for supplying the first voltage to the first conductor wire, and the first peripheral apparatus being connected to receive a second voltage on a second conductor wire of the USB, the method comprising:

detecting in the first peripheral apparatus the second voltage received on the second conductor wire of the USB;

storing in the first peripheral apparatus a logic value corresponding to a presence or an absence of the second voltage; and

operating the supply voltage source only if the stored logic value indicates that the second voltage is present based upon a comparison with the stored logic value using a logic circuit, to protect the second peripheral

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apparatus from receiving the first voltage via the first conductor wire of the USB when the second voltage is not present.

23. (Previously presented) A method according to Claim 22, wherein the detecting comprises:
generating an output signal from a Schmitt trigger having an input connected to the second conductor wire of the USB;
detecting a rising edge or a falling edge of the output signal, and producing at least one signal corresponding to the detected rising and falling edges of the output signal;
counting a duration from which a logic value of the detected rising edge or of the detected falling edge of the output signal is maintained, and for producing an end of count signal when the counted duration reaches a predetermined value; and
using a state machine for changing logic states as a function of the detected rising edge and the detected falling edge of the output signal and as a function of the end of count signal, the state machine for producing a signal having a logic value corresponding to the presence or absence of the second voltage and for producing a signal indicating that the logic value corresponding to the presence or absence of the second voltage has changed.

24. (Previously presented) A method according to Claim 22, wherein the first peripheral apparatus comprises a state register comprising at least one latch; and wherein the logic value corresponding to the presence or absence of the second voltage is stored in the at least one latch.

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25. (Previously presented) A method according to Claim 22, wherein operating the supply voltage source comprises:

inverting the logic value corresponding to the presence or absence of the second voltage; and
using a NOR circuit having a first input for receiving the inverted logic value corresponding to the presence or absence of the second voltage, and a second input for receiving a logic value indicating that the supply voltage source can be operated.

26. (Previously presented) A method according to Claim 22, wherein the first peripheral apparatus comprises a microcontroller, an interrupt state register (ISR) for the microcontroller and comprising a plurality of latches, and an interrupt mask register (IMR) for the microcontroller and comprising a plurality of latches; and wherein the method further comprises:

interrupting the microcontroller by
recording in the at least one latch from the ISR a change in the logic value corresponding to the presence or absence of the second voltage,
recording in the at least one latch from the IMR whether the microcontroller requires knowledge of the logic value recorded in the at least one latch from the ISR, and
using an AND circuit having a first input connected to the at least one latch from the ISR and a second input connected to the at least one latch from the IMR, for providing at an output an interrupt request signal to the

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microcontroller only if there occurs a change in the logic value corresponding to the presence or absence of the second voltage and if the logic value recorded in the at least one latch from the ISR has a 1 logic value.

27. (Previously presented) A control device according to Claim 7, wherein said first peripheral apparatus further comprises a microcontroller; and wherein said detection circuit detects the second voltage received on the second wire of the USB during a predetermined time period.

28. (Previously presented) A first peripheral apparatus according to Claim 13, further comprising a microcontroller; and wherein said detection circuit detects the second voltage received on the second wire of the USB during a predetermined time period.

29. (Previously presented) A method according to Claim 22, wherein said first peripheral apparatus further comprises a microcontroller; and wherein said detecting comprises detecting the second voltage received on the second wire of the USB during a predetermined time period.